SOC H.265/HEVC Video/Audio Encoder IP Core Datasheet

(Integration information is provided in the IP core Integration Sheet)

System-On-Chip (SOC) Technologies

1. Product Overview

The SOC H.265 HEVC video encoder IP core is a single chip solution, which is designed to support single or multi-stream H.265 video encoding for all industrial standard resolutions including QVGA, SD, HD up to 1080p@120, and 4K@60 (8K@60 will be supported). It currently supports up to1080@60, and 4K@60. Higher resolutions will be released in the near future.

The SOC H.265 video encoder IP core supports FPGAs of both Xilinx and Intel. SOC also supplies all-in-one encoder modules based on the same H.265 video encoder IP core. Refer to the Product Brief and Datasheet for SOC MPEG codec modules for details.

The SOC-Mcodec Chipsets are “ASICs” based on FPGAs and SOC codec IP cores, which allow the customers to drop on their PCB exactly the same way as traditional ASICs, but with advantage of upgradable. Refer to the Product Brief and Datasheet (Chip Selection Sheet) for details.

The SOC H.265 HEVC video encoder is implemented based on SOC’s proprietary single-clock driven all-hardware technology (without microprocessors or embedded software), which has significant advantages of high-speed (low latency), small footprint (low power), high video quality, and high resolution. The encoder can fit into a mid-end FPGA, for example, the XiIinx Zynq-7000 series and the Intel Arria-10 series.

The SOC H.265 HEVC video encoder (all of the versions) is at Main 4:2:2, 10bits. The encoder encodes either 4:2:0 or 4:2:2 streams whichever is desirable. The encoder supports both 8-bit and 10-bit profile (12 bit will be available). The 8-bit encoder is most suited for consumer products, while the 10-bit version is for high-end applications such as broadcast, digital cinema, and medical devices.

The SOC H.265 HEVC video encoder comes with a user API which allows the user to control the operations of the encoder, including CBR or VBR, bit rate, etc. The API user manual is shipped with the evaluation and product development kit.

The H.265 encoder IP core is customized into the following versions:

1. Standard Version:
   A balanced system optimized for key factors of logic resource utilization and performance.

2. I-Frame Version:
   The I-frame version implements intra-prediction (I-frames) only, without motion vector predictions, which reduces the logic reduces logic resources and simplifies decoder complexity.

3. Slim Version:
   The slim version encoder is optimized for low logic resources, which uses about 50% of the logic resources compared to the standard version.

Other special versions of the SOC H.265 video encoder, such as multiple channels and dual core for 3D HD TVs, are also available. Please contact SOC for product details.

The SOC H.265 HD, 4K, and 8k H.265 encoder IP cores are released as separated products.

The SOC encoder series can be integrated with an audio encoder to provide an all-in-one encoding solution. Two solutions are available:

1. FPGA+DSP with the external DSP for audio encoding;
2. A single chip solution using FPGAs that have an ARM processor, such as the Xilinx Zynq-7 series and Intel Arria-10 FPGAs. The SOC MPEG encoder IP cores can be licensed for either video or audio only or both video and audio encoding as a system.

The MPEG Transport Encoder (multiplexer) is usually included in an encoder IP core. SOC also provides network modules, TCP/UDP-IP, Ethernet MAC IP cores, which can be licensed along with the H.265 video/audio encoder IP cores. Customized versions of these products are available on request.

A video scaler is also available, which can scale the input video into any standard resolutions before encoding. The video scaler can also output multiple scaled videos (1-7 videos) for multiple streaming. SOC also provides integration services for its customers. Contact SOC sales, sales@soctechnologies.com, for information.

Note: Information for Integrating the H.265/HEVC IP core into a user system is provided in the H.265 IP Core Integration Sheet

2. The SOC H.265 HEVC Video Encoder Architecture

Fig. 1 is the block diagram of the SOC H.265 HEVC video encoder. It is a self-contained FPGA IP core that can be either placed into a single FPGA or integrated with other logic blocks in the same FPGA for system-on-chip solutions.

All of the blocks in the design, shown in Fig. 1, are implemented in hardware without embedded processors or embedded software. It offers high speed, low logic resource consumption, and low power. Input to the encoder is standard raw video stream in either 4:2:0 or 4:2:2 format. The output of the encoder is H.265 elementary stream. SOC also provides an MPEG transport encoder to allow the output of the encoder to be in the form of MPEG transport streams.

The SOC H.265 video encoder requires two external clock sources, one at 100MHz and the second at the video clock frequency (13.5-148.5MHz). The encoder also requires an external DDR3 (or DDR4) memory of minimum of 256MB for 1080p resolution (for both 30fps and 60fps).

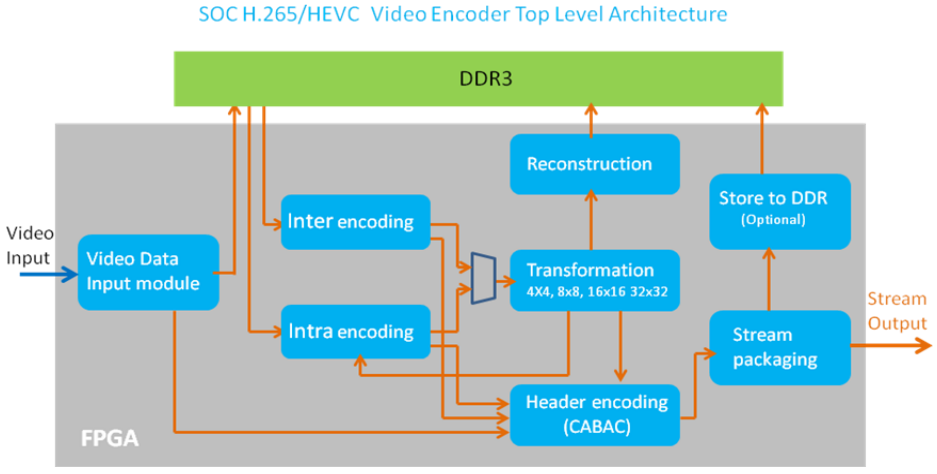

Fig. 1 Block Diagram of SOC H.265 HEVC video encoder

3. The H.265 HEVC and AAC Video/Audio Encoder Solutions

SOC provides two H.265 and AAC video/audio encoder solutions:

(1) FPGA-DSP solution – for FPGAs that do not have an embedded ARM processor, an external DSP is used for audio encoding. Fig. 2 shows the architecture. The audio signal is sent to the external DSP (the Blackfin BF512) for encoding. The encoded AAC stream is sent back to the FPGA, which is encoded into the transport stream by the transport encoder in the FPGA.

(2) Single FPGA Solution – for FPGAs that have the ARM embedded processors, the ARM processor is used for audio encoding. The video encoder IP core uses the logic part of the FPGA. Fig. 3 provides a block diagram for this single chip solution.

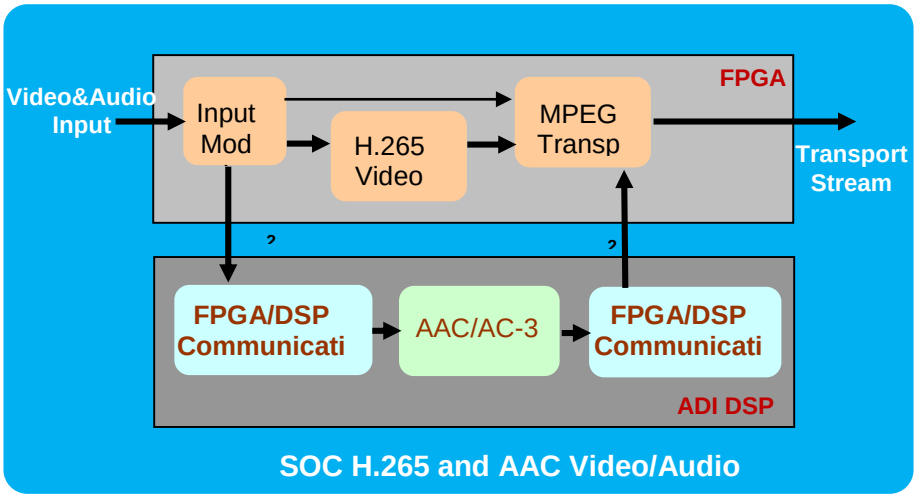

Fig. 2 Block Diagram of FPGA-DSP video/audio encoder solution

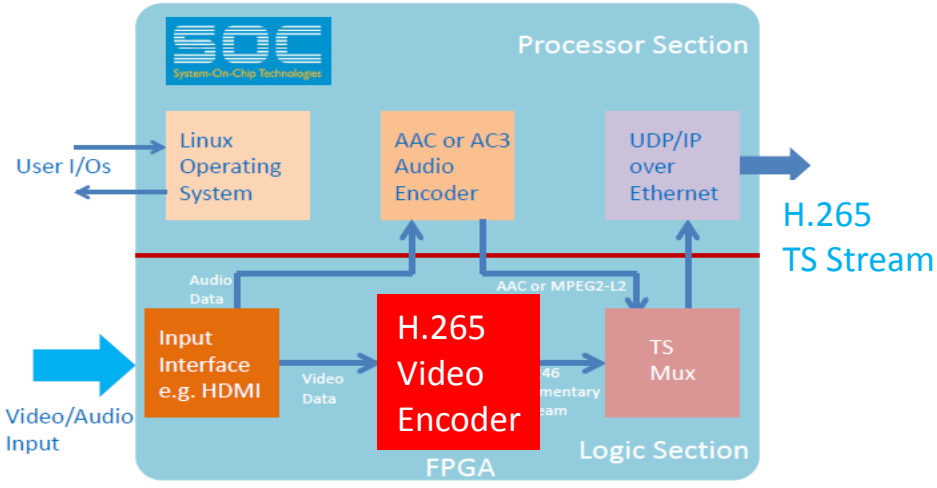

Fig. 3 Block Diagram of Single FPGA video/audio encoder solution

4. Technical Specifications

Conformance Standard:

- Video: H.265/HEVC (ISO/IEC 23008-2:2015)
- Audio: HE-AAC (ISO/IEC 14496-3)

Profiles:

The SOC H.265 video encoder supports:

- Main 4:2:2 10

Chroma Format:

- 4:2:0
- 4:2:2

Precision:

- 8 bits
- 10 bits

Frame Rate:

- 10fps
- 24fps
- 25fps
- 29.97fps
- 30fps
- 50fps
- 59.95fps
- 60fps
- 120fps

Inter Frames:

The SOC H.265 video encoder supports:

- I frame
- I&P frame

Audio Sample Rate:

- 32kHz, 44.1kHz and 48kHz.

Audio Bit Rate (total for all channels in v2 stereo encoding mode):

- 16-18 kbps (32 kHz), 16-36 kbps (44.1 kHz and 48 kHz).

Latency:

- Standard Version: 0.25ms for HD, 0.5ms for 4k.

Output Stream Format:

- Constant Bit Rate (CBR) – User controllable through API
- Variable Bit Rate (VBR) – User controllable through API.

Logic Resource Consumption (Xilinx FPGAs):

- Standard Version: 200k LUTs, 10Mb of Block RAM, 630 DSPs
- I-Frame Version: 140k LUTs, 3Mb Block RAM, 630 DSPs

Logic Resource Consumption (Intel FPGAs):

- Standard Version: 150kALMs, 10Mb of Block RAM, 630 DSPs
- I-Frame Version: 110kALMs, 3Mb Block RAM, 630 DSPs

Power (Core only):

- Standard Version: 2.5w (core only)
- I-Frame Version: 1.5w (core only)

5. Targeted FPGAs

The SOC H.265 video encoder fits most of the Xilinx FPGAs, including:

- Kitex-7
- Zynq-7
- Ultrascale
- Virtex-7

Encoder IP cores are also available for Intel FPGAs, including:

- Arria-10
- Stratix-V

6. Applications

- Broadcast Equipment
- Satellite video/audio transmission equipment
- Cable TV headend
- Medical imaging devices
- IPTVs distributing
- Video surveillance cameras
- Video conferencing devices
- Digital cinemas.

7. Product Formats

SOC provides three formats to customers, which allows ease-of-use of the product. These formats include:

1. FPGA IP cores

   Self-contained IP cores for FPGA users, in either bit file or encrypted netlist. An integration datasheet will be provided with the delivery of the netlist.

2. SOC MPEG Codec Modules

   SOC provides all its codecs on small circuit boards that integrates all required components for video, audio or both video and audio encoding. The codec module connects to a host device via a PCB connector. SOC also provides evaluation/development boards.

3. Chipsets – The SOC-Mcodec

   The SOC codec chipsets, SOC-Mcodec, are FPGA based ASICs. The SOC IP cores are used to configure the chipsets. The SOC-Mcodec offers a convenient way for customer product production.

4. Customized system-on-chip solutions surrounding the encoder
   SOC provides integration with other IP cores to produce a system-on-chip solution.

Technical data for using each of the above formats are described in the following Sections.

8. H.265 Video Encoder IP Core Integration Sheet

When the encoder is delivered in IP core format, it is a ready-to-use "netlist" core for FPGAs. Fig. 4 shows the inputs and outputs of the encoder core.

The H.265 video encoder IP core integration details are provided in a separate document under the title of "H.265 Video Encoder IP Core Integration Sheet".

Fig. 4 The inputs and outputs of the H.265 video encoder IP Core

9. SOC MPEG Codec Modules

SOC supplies all its MPEG2, MPEG4-AVC/H.264 and H.265/HEVC encoders and decoders on a 2.7"x2.0" or 2.7"x2.5" module (card), as shown in Fig. 5. The modules provide complete function of video/audio encoding or decoding. The module connects to the host product/PCB via a device-to-PCB connector, as shown in Fig. 6.

Refer to the Product Brief and Datasheet of SOC MPEG Codec Modules for technical details.

Fig. 5 SOC MPEG Codec ModuleS

Fig. 6. Device-to-PCB connector

The SOC MPEG Codec Modules can be directly connected to I/O interface chips for product fabrication, as shown in Fig. 7, or connected to an FPGA or a Microcontroller for user system integrations, as shown in Fig. 8.

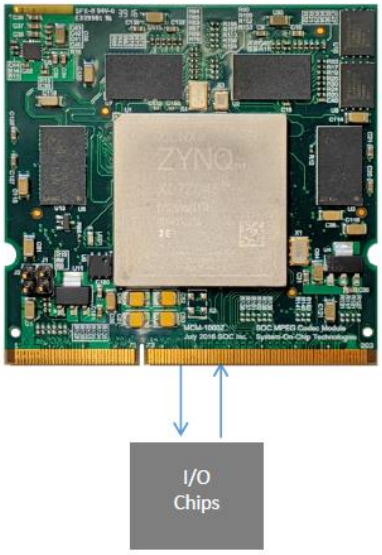

Fig. 7 SOC MPEG Codec Module directly connects to I/O interfaces in user product

Fig. 8 SOC MPEG Codec Module connects to FPGA/microcontroller for user integration

10. The H.265 Encoder Chipset

SOC Technologies provides a series of CODEC chipsets, the SOC-Mcodec family, which can be dropped onto user PCBs as ASIC video encoders and decoders. The SOC-Mcodec family of chipsets support all MPEG standards, including H.265, H.264, and MPEG-2, and all industrial standard resolutions, including SD, 720, 1080, 4K, and 8K, with frame rates of up to 120 fps.

The SOC H.265 HD Encoder Chipset includes an FPGA and FLASH preconfigured with SOC's H.265 HD Encoder IP Core. It is an ASIC that receives raw video/audio and outputs an H.265 video stream with optional AAC/MP2/MP3 audio compression. It supports resolutions up HD at 120 fps

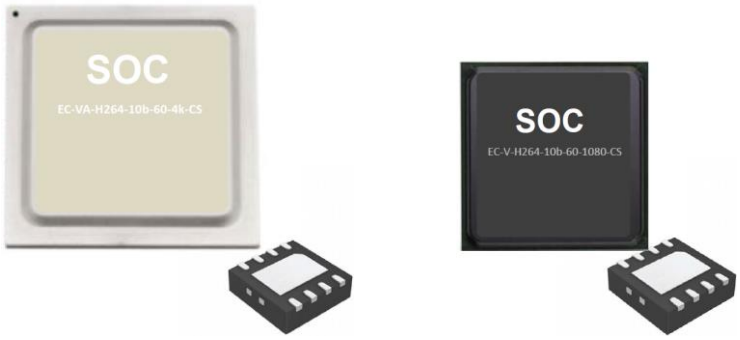

Fig. 9 SOC-Mcodec chipsets

SOC CODEC Chipsets are fully pre-configured FPGA chips that are designed to function just like traditional ASIC chipsets, integrated onto user PCB by connecting the pins.

The Chipset I/O interfaces can be customized to virtually any customer specifications, making them the most flexible CODEC chipsets on the market. This is especially useful if your system demands non-standard I/O interfaces - let us tailor the interfaces to work in harmony with your system. Unlike traditional ASICs, SOC's CODEC chipset firmware may be updated to change its functionality or I/O interfaces if needed.

The SOC CODEC Chipsets are built using SOC Technologies' portfolio of ultra-high-performance CODEC and peripheral IP Cores. You can expect high quality, high speed, low latency, and low power-consumption.

With high volume productions of FPGAs, today's FPGAs are fabricated using the most current silicon technologies that are used for computer CPUs, such as the new 10nm silicon class. This makes the FPGA-based ASICs ahead of the traditional MPEG codec ASICs, in power consumption, speed and cost.

11. Customized System-on-Chip Solutions Surrounding the Encoder

SOC also provides customized system-on-chip integrations based on the H.265 video/audio encoders. Fig. 10 shows an example of an integrated encoder solution for HD video over the Internet with HDMI input.

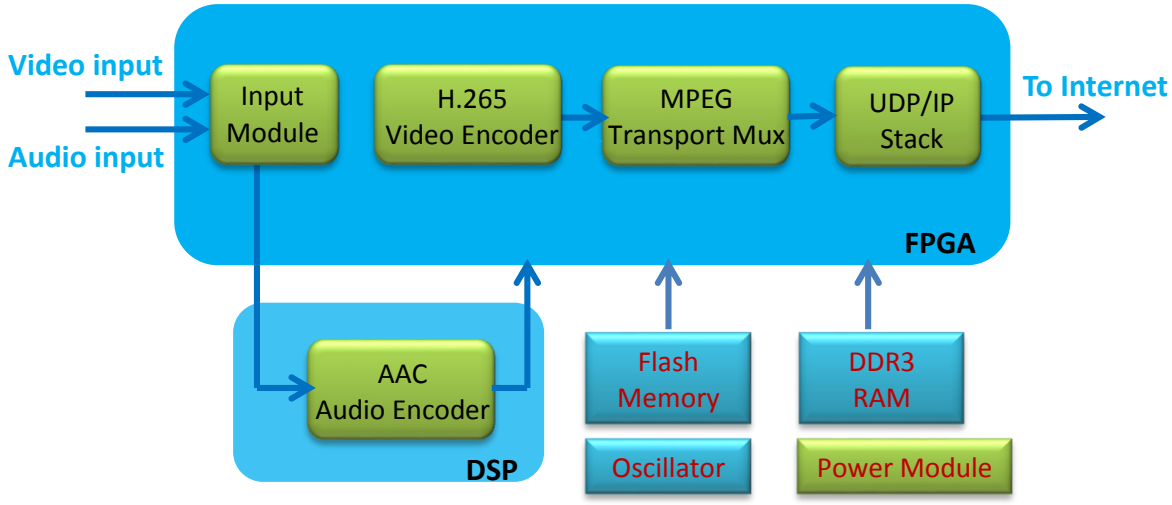

Fig.10 Example system-on-chip solution – HD-over-IP encoder

12. User API

The encoder (IP core or module) is controllable through a user API, which allows the user to control the operations of the encoder through setting the control registers at runtime. Refer to the "H.265 Video/Audio Encoder API Manual" for details.

13. Related Documents

1. Integration Sheet – Encoder IP Cores
2. API Manual – H.265 Encoder IP Core
3. Datasheet – Encoder Modules
4. Datasheet – Encoder Chipsets

14. Technical Support

SOC provides technical support for all its products, which includeS documentation, e-mail based, and telephone based support. Additional support services, such as on-site training services, can be subscribed from SOC as a service contract.

15. IP core upgrading

Upgrades to the IP core are available to all the delivery formats discussed in Sections 6. Upgrade is usually a part of the technical support contract signed individually. On-line automatic upgrading can also be arranged if desirable.

16. Ordering Information

The SOC H.265 video/audio encoder IP cores are available for licensing, or one-time fee purchase, or a combination of one-time fee plus reduced royalty payments.

The SOC H.265 video/audio encoder module is A complete solution for video and audio encoding at low cost. It is sold on unit by unit basis.

SOC also provides integration of the H.265 encoder with other functional IP cores of SOC or customer provided IP cores. A combination of NRE and licensing royalties is normally considered, which is negotiated on case by case basis.

Please contact SOC sales by telephone +1 519 880-8609 or e-mail: sales@soctechnologies.com

17. Document Revisions

Version #	Revision Date	Notes
V.1.0	2015/08/15	First release
V.1.1	2016/04/10	
V.1.2	2016/10/21	
V.2.0	2019/08/10	Major Revision